



**BEST AVAILABLE COPY**

(19) Generated Document. (11) Publication number: **08242006 A**

**PATENT ABSTRACTS OF JAPAN**

(21) Application number: **08032979**  
 (22) Application date: **27.01.96**  
 (51) Int. Cl.: **H01L 29/786 H01L 21/336 H01L 27/12**

(30) Priority:	(71) Applicant: <b>SEMICONDUCTOR ENERGY LAB CO LTD</b>
(43) Date of application publication: <b>17.09.96</b>	(72) Inventor: <b>YAMAZAKI SHUNPEI</b>
(84) Designated contracting states:	(74) Representative:

**(54) PRODUCTION OF  
SEMICONDUCTOR DEVICE**

(57) Abstract:

**PURPOSE:** To obtain a high performance by forming a true non-single crystal semiconductor layer on a silicon oxide film that is formed by a low-pressure CVD method using disilane or trisilane and crystalizing it at a specific low temperature.

**CONSTITUTION:** A silicon oxide film is formed as a blocking layer 51 on a glass 50 that is inexpensive such

as quartz glass, etc., and can withstand the heat treatment of at most 700°C, by using a high frequency sputtering method. A disilane or trisilane is supplied through for film formation by a low pressure vapor method at 450-550°C that is 100-200°C lower than the crystallization temperature. Then, after a silicon film in an amorphous state is formed, it is entirely annealed in an atmosphere of non-oxide for 12 to 70 hours at an intermediate temperature of 450-700°C, and a silicon film 52 is changed from an amorphous structure to higher-order state, thereby obtaining higher carrier mobility without grain boundary. The film 52 is subjected to photoetching, and an area 22 for a PTH is formed on the right side of the glass 50 and an area 13 on the left side thereof, respectively, then gate electrodes 55 and 56 are formed thereon by using the silicon oxide film as a gate insulation film 54.

COPYRIGHT: (C)1996, JPO



